MMIC 14-GHz VCO and Miller Frequency Divider for Low-Noise Local Oscillators

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Abstract—An MMIC voltage-controlled oscillator and an MMIC frequency divider are developed and applied to a 14-GHz low-noise local oscillator. To obtain both wide tuning range and low pulling figure, the source-follower FET circuit is used in the voltage-controlled oscillator. A wide-band balanced mixer and a filtering amplifier are integrated in a single chip and constitute the Miller frequency divider. The MMIC's were assembled into a 14-GHz phase-locked loop in order to demonstrate that they will operate as key components of low-noise oscillators. It is shown experimentally that even for low-Q MMIC circuitry, the carrier noise of the oscillator is reduced enough for practical purposes such as space-borne heterodyne receivers, transmitters, and radio repeaters in *Ku*-band satellite communication systems. Thus, prospects are bright for development of single-chip microwave low-noise oscillators.

I. Introduction

MINIATURIZATION of stabilized microwave oscillators is an important aspect in developing small-size, lightweight equipment for microwave communications. Several kinds of monolithic microwave integrated circuits (MMIC's), including voltage-controlled oscillators (VCO's) and frequency dividers, have been developed for phase locked loop (PLL) applications [1]–[4]. However, to date practical microwave PLL's have employed hybrid circuitry [5]. There are at least two problems in developing an MMIC PLL. Solution to these two problems is the main subject of this paper.

One is how to stabilize the oscillation and reduce oscillator carrier noise that occurs because of the fairly low Q monolithic circuitry. A typical GaAs MMIC VCO exceeds -80 dBc/Hz in SSB noise power density at 100 kHz off from the carrier [1]. Communication systems in most cases require the same noise density at only 1 kHz off from the carrier. Considerable noise reduction is necessary in order to satisfy this requirement. Phase locking to a X'tal oscillator by a PLL is a possible solution, but it may take a fairly high loop gain to reduce the noise drastically. Such high gain may be dangerous in a loop at microwave frequencies. Experiments must be conducted to determine whether the PLL approach can be used with a MMIC VCO for noise reduction.

The other problem concerns the development of a frequency divider in the MMIC. The VCO signal should be divided in frequency down to the X'tal frequency (usually 10–100 MHz). There are two categories of frequency dividers. One comprises digital frequency counters. Recent GaAs FET or Si bipolar logic technology has provided very high speed divider IC's [6], [7]. They are capable of broad-band performance, but they are confined to X-band frequencies or lower. The other category comprises analog frequency dividers. The concept of analog frequency division was first proposed by Miller as fractional-frequency generation utilizing regenerative modulation [8]. Since then, several kinds of analog frequency dividers have been developed in hybrid IC configurations [9], [10]. The prototype MMIC Miller frequency divider discussed here was developed by the authors. The design, construction, fabrications, and basic performance of the divider have already been reported [2]. For applications to the PLL, the divider must be examined in terms of input-to-output carrier noise performance.

This paper describes the development of the MMIC VCO and Miller frequency divider, and their trial applications in a 14-GHz PLL. It is shown experimentally that the oscillation frequency is stabilized by locking to a VHF reference oscillator. Noise reduction performance is presented as a function of the loop gain of the PLL.

II. Voltage-Controlled Oscillator (VCO)

Monolithic circuits have fairly low Q factors, resulting in MMIC oscillators having parasitic oscillations. The oscillation frequency is susceptible to the device parameters and the load impedance. Moreover, frequency trimming cannot be carried out after fabricating the MMIC. Therefore, these circuits must be designed taking tuning ranges and pulling figures into account.

A VCO composed of an FET, variable reactance, and an output port leading to the load is realizable in six basic arrangements, as shown in Fig. 1. Oscillation may take place only when the magnitude of the output port reflection coefficient is greater than unity. The output port reflection coefficient Γ_o is related to the variable reactance reflection coefficient Γv as

$$\Gamma_o = S_{11} + \frac{S_{21}S_{12}\Gamma v}{1 - S_{22}\Gamma v}$$

where S_{11}, S_{21}, S_{12}, and S_{22} are the S parameters of the FET in each arrangement shown in Fig. 1 [11]. Applying

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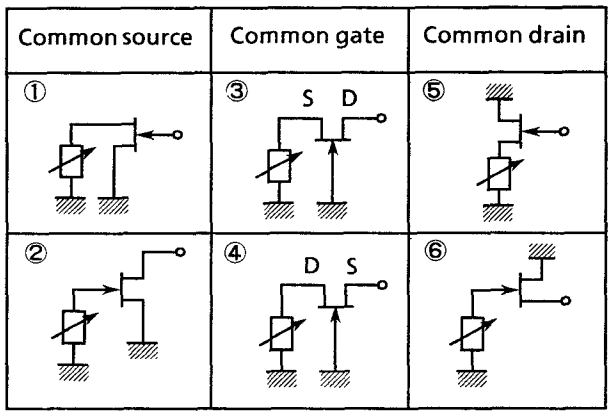


Fig. 1. VCO circuit configurations.

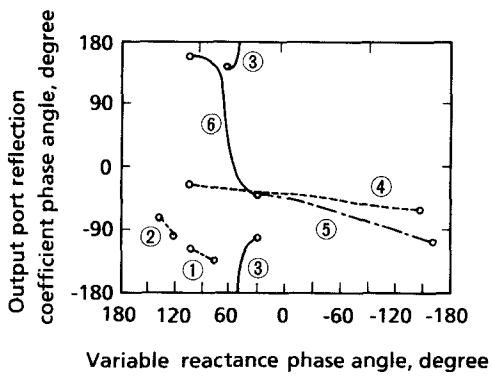


Fig. 2. Output port reflection coefficient phase angle versus variable reactance phase angle.

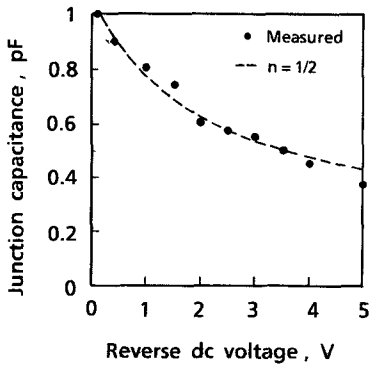


Fig. 3. Varactor response.

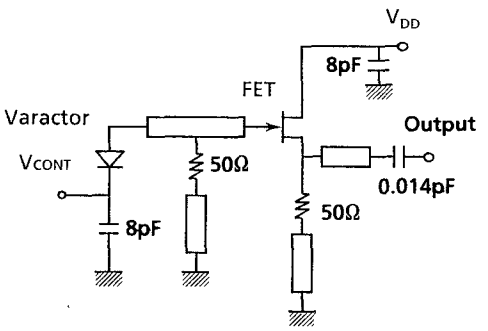


Fig. 4. VCO circuit diagram.

the above formula to a commonly used 0.5×280-μm-gate GaAs MESFET, the output port reflection coefficient was calculated numerically, where the small-signal S parameters of the FET measured at 14 GHz in the dc bias condition of 3V–10mA were used. The calculated phase angle of the output port reflection coefficient is shown in Fig. 2. In this figure, the phase angle is depicted only in the range where the output port reflection coefficient magnitude exceeds unity. The oscillation frequency is determined by Γ_o and the load impedance. Since the load impedance is fixed, the oscillation frequency varies more as Γ_o varies more. Therefore, the source-follower common-drain circuit ⑥ should be used in order to obtain wide tuning ranges with small variable reactance changes. With this circuit, oscillation may take place when the variable reactance is in the 30–110° inductive range.

A planar Schottky-barrier diode is suitable for monolithic integration with MESFET's and is used here as the variable capacitor. Since the MESFET has a 0.5×280-μm gate, as mentioned above, a Schottky-barrier diode with 0.5×280-μm stripe is especially suitable for the fabrication process with the MESFET. The 0.5×280-μm-stripe diode was tuned from 1.0 to 0.5 pF in junction capacitance by applying the reverse dc bias of 0 to 5 V, as shown in Fig. 3. This junction curve has a gradient of one in two ($n=1/2$). Since the variable reactance to be used here should be inductive for oscillation, the capacitive Schottky-barrier diode must be coupled via an impedance transformer.

Based on the above factors, the circuit design was carried out. The resultant circuit diagram of the MMIC VCO is shown in Fig. 4. The above-mentioned varactor diode was coupled to the gate of the common-drain FET via a quarter-wavelength microstrip impedance transformer. A 50-Ω resistor was inserted into the FET source for autobiasing and drain current stabilization. Another 50-Ω resistor was connected to the microstrip impedance transformer at the RF zero voltage point. These resistors function not only as biasing circuits but also as Q-damping elements to prevent parasitic oscillations. For frequencies much lower than the oscillation frequency, the diode appears to be open and the microstrip looks much shorter than a quarter wavelength, so that the FET sees only the 50-Ω resistor. For frequencies much higher than the oscillation frequency, the diode is reduced in Q value and the FET is also reduced in gain. Therefore, no possibility exists for the circuit to exhibit any parasitic oscillations at out-of-band frequencies. The output coupling capacitor is small enough to reduce the pulling figure. The coupling coefficient is about -17 dB at 14 GHz.

The VCO was implemented on a $2\times2\times0.15$-mm GaAs chip, as shown in Fig. 5. Fig. 6 gives the performance of the fabricated MMIC VCO measured with an FET dc bias of 3 V by 10 mA. The VCO is tunable smoothly from 11.3 GHz to 14.3 GHz by the 0–7-V control voltage on the diode. The output power is approximately -4 dBm, which is rather low because of the weak output coupling. Taking into account the -17-dB coupling coefficient and dc power dissipation of the FET, the oscillation efficiency is reasonably calculated at 10–20 percent. The pulling figure was measured by using a coaxial variable load, where the

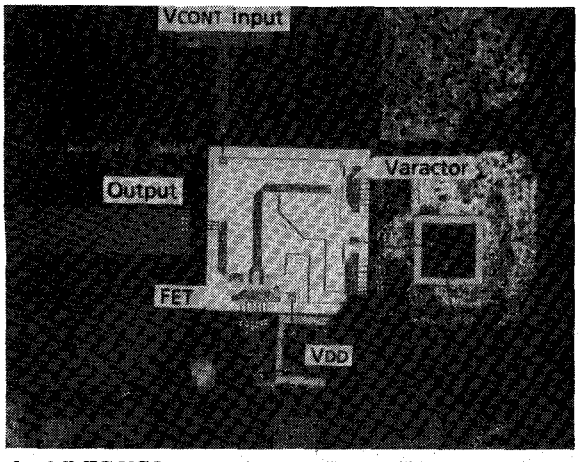


Fig. 5. MMIC VCO mounted on test fixture. Chip size: 2 mm×2 mm.

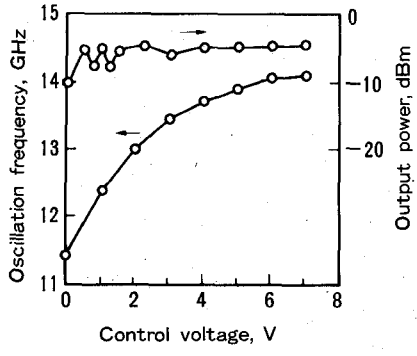


Fig. 6. VCO frequency and output power.

VCO was loaded with a coaxial sliding short through a 3-dB attenuator. The oscillation frequency varied ±30 MHz around the center frequency as the sliding short was moved. The free-running spectrum of the VCO is shown in Fig. 7, where RESBW and VBW stand for the resolution band width and the video filter band width of the spectrum analyzer. No parasitic oscillation was found over the frequency range of 2 to 22 GHz. The line width of the spectrum was about 1 MHz. The free-running short-term frequency stability was about 10^{-3} to 10^{-4}. The spectral purity and the frequency stability were fairly low because of the low-Q monolithic circuitry, and not good enough for many practical communication purposes. This VCO cannot be used in free run, but is used with a phase locked loop. The phase locked loop provides a much better spectral purity and frequency stability, as discussed in the following chapters.

III. Miller Frequency Divider

A prototype MMIC Miller frequency divider has been developed. Its design, fabrication, and basic performance have already been reported by the authors [2]. Here, we will review it briefly. The Miller frequency divider is a down-converter with a feedback loop consisting of a balanced mixer and a filtering amplifier, as shown in Fig. 8. Amplifier gain should be high enough to compensate for the conversion loss of the mixer, and the RF/IF leakage of the mixer should be low enough to avoid self-oscillation in the feedback loop [12]. To obtain high RF/IF isolation, the mixer must maintain its balance over a wide frequency range. To accomplish this, two mixer diodes were arranged close to each other on the chip. In addition, an interdigitated quadrature coupler (Lange coupler) was employed in order to constitute the wide-band 180° hybrid ring, as shown in Fig. 8. In this configuration, an RF/IF isolation exceeding 15 dB was obtained from dc to 9 GHz IF range. This frequency divider operated at 14 GHz with 800-MHz bandwidth [2].

Before applying the developed divider to the PLL, we shall examine the divider in terms of input-to-output carrier noise performance. The carrier noise of the VCO signal is due to fine fluctuations of the oscillation frequency. For proper PLL operation to occur, the frequency fluctuations should be transferred precisely to the phase comparator via the frequency divider.

The divider mounted on a test fixture and the setup for measuring carrier noise performance are shown in Figs. 9 and 10, respectively. The input 14-GHz signal with some carrier noise was divided into 7 GHz, and the input and output carrier noise was measured with a very clean reference oscillator. The measured carrier noise spectrum in the input and output signal is shown in Fig. 11. The resultant data show that carrier noise was suppressed by 4–8 dB in the range 1 kHz to 1 MHz off the carrier and increased slightly in the farther range. An ideal divide-by-two Miller frequency divider without in-loop delay would theoretically provide FM deviation suppression of 6 dB [12]. The measured data agree fairly well with the theory.

IV. Phase Locking and Noise Reduction

The MMIC VCO and Miller frequency divider described above were tested for a 14-GHz PLL. The trial PLL was composed of the VCO followed by a buffer amplifier, a Miller frequency divider, a digital 1/64 frequency divider, a phase comparator, and other circuitry, as shown in Fig. 12. The digital 1/64 frequency divider consisted of six cascaded 1/2 dividers using a BFL (buffer FET logic) gate dynamic divider in the head stage and static dividers in the second through sixth stages [6], [7]. An EXCLUSIVE-OR gate followed the 1/64 divider and compared the phase of the divided signal with the phase of the external reference signal. A synthesized signal generator was used as the reference oscillator instead of an X'tal oscillator. The reference frequency was 109.375 MHz (=14.0 GHz÷2÷64).

The EXCLUSIVE-OR gate output signal drives the VCO through a dc amplifier and filters. The band-reject filter was tuned in order to eliminate the reference signal. The low-pass filter had a lag–lead phase characteristic which filtered the reference signal harmonics and high-frequency residual noise in the reference signal.

The low-pass filter should be adjusted to minimize the total output noise power. Noise performance of the free-running VCO was measured and was indicated by the short dashed line in Fig. 13. The reference oscillator noise

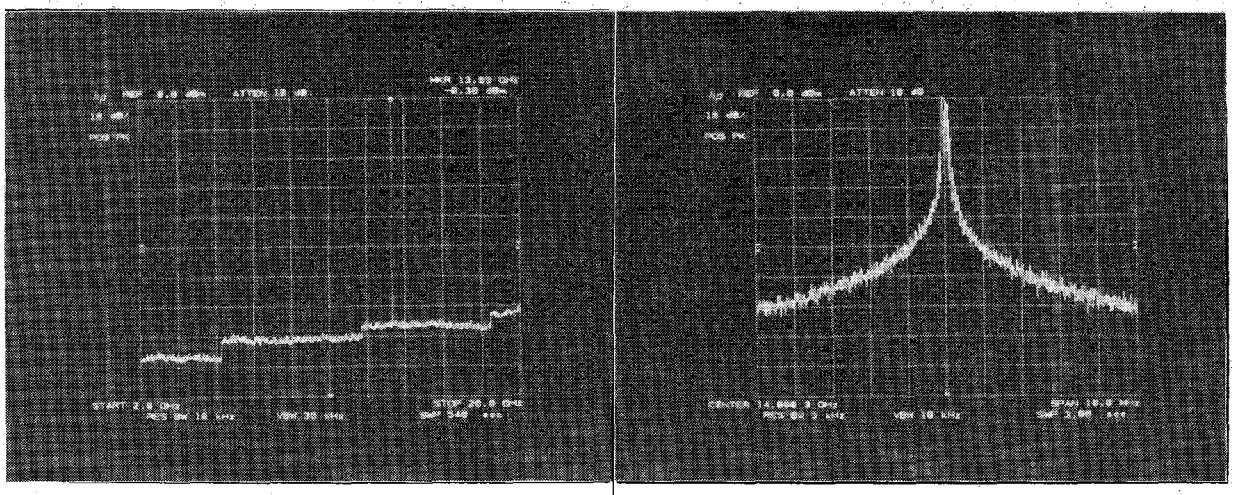


Fig. 7. Free-running oscillation spectrum. (a) Wide range spectrum. (b) Near carrier spectrum.

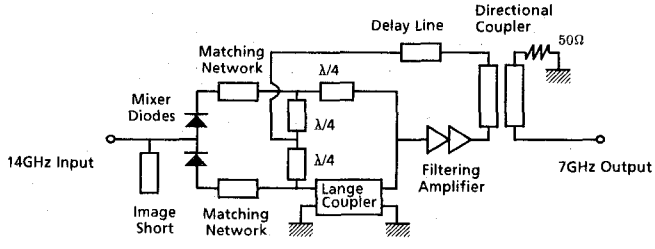


Fig. 8. Miller frequency divider configuration.

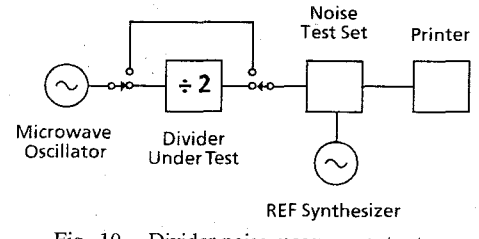


Fig. 10. Divider noise measurement setup.

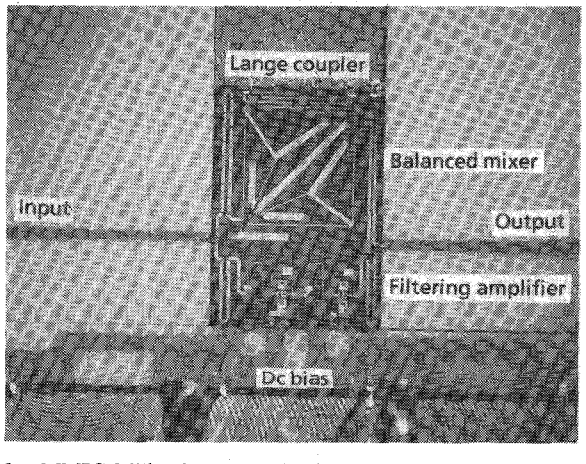


Fig. 9. MMIC Miller frequency divider mounted on test fixture. Chip size: 4.8 mm × 6.75 mm.

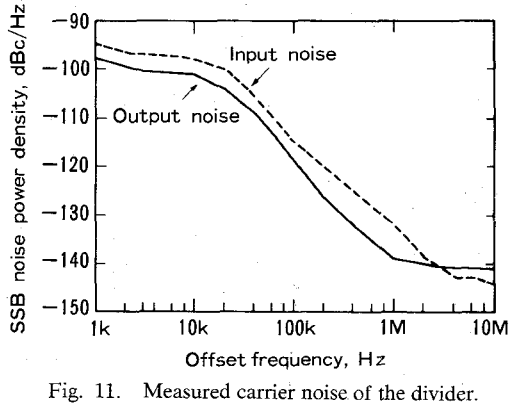


Fig. 11. Measured carrier noise of the divider.

level was converted form the reference frequency (109.375 MHz) to the microwave frequency (14.0 GHz) by adding 42 dB, as indicated by the alternate long and short dashed line. These two lines cross at 1 MHz off from the carrier. Therefore, the cutoff frequency of the low-pass filter was adjusted to this cross point frequency.

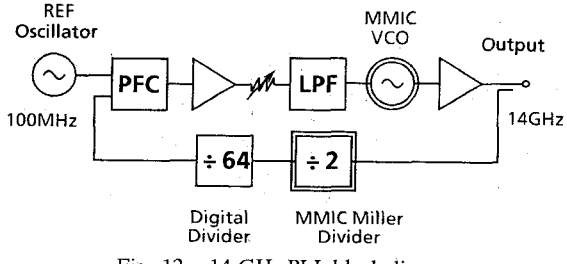


Fig. 12. 14-GHz PLL block diagram.

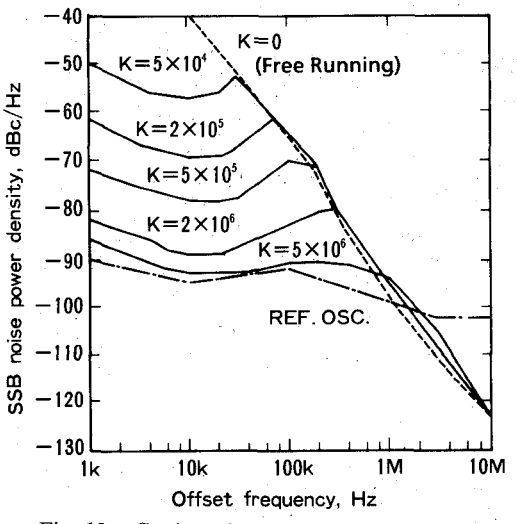
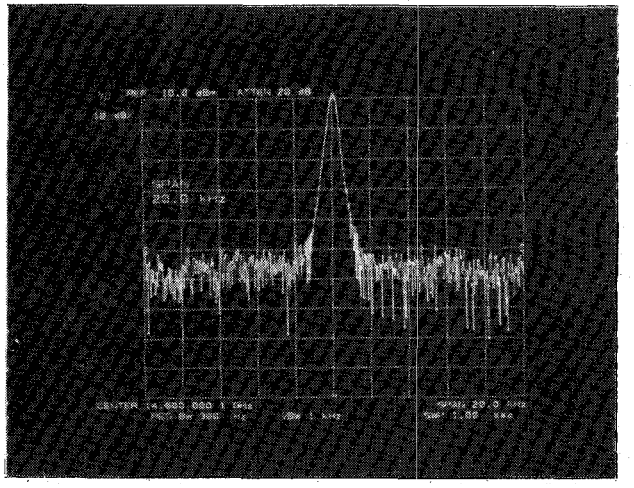


Fig. 13. Carrier noise performance of the PLL.

Another key parameter that influences output noise is the loop gain of the PLL. The loop gain was controlled by a variable attenuator inserted between the dc amplifier and the low-pass filter. The spectrum of the PLL is shown in Fig. 14. The measured noise distribution for various values of the loop gain is depicted by the solid lines in Fig. 13. The noise level near the carrier decreases with increasing loop gain. As a matter of course, the noise reduction is limited to the reference oscillator noise level (alternate long and short dashed line). The loop gain of 5×10^6 [s^{-1}] is necessary and sufficient for noise reduction within the above limitation. This high loop gain reduces carrier noise to less than -80 dBc/Hz at 1 kHz off from the carrier center.

V. Conclusions

An MMIC VCO and Miller frequency divider were developed and tested for a 14-GHz PLL. The VCO was designed to have sufficient tuning range to compensate for the frequency drift caused by fluctuations of device parameters or the load impedance. Using a common-drain source-follower circuit, a tuning range of 3 GHz and a pulling figure of ±30 MHz were obtained in the 14-GHz band. An integrated microstrip impedance transformer with a Q-damping bias line was also employed in order to prevent parasitic oscillations in the VCO. No parasitic oscillations were found throughout the 2–22-GHz frequency range. The MMIC Miller frequency divider was found to have no serious additional noise. The measured noise data agreed fairly well with a simple theoretical prediction. It was confirmed experimentally that the carrier noise, one of the most serious parameters of the MMIC oscillator, was reduced by increasing the loop gain of the PLL. Carrier noise reduction to -80 dBc/Hz (1 kHz offset from carrier) was obtained. This was close to the reference oscillator noise level and is regarded as low enough for local oscillators in most communication systems.



V:10dB/div
Center:14GHz,Span:20kHz
RESBW:300Hz,VBW:1kHz

Fig. 14. Phase-locked oscillation spectrum.

This study demonstrated that the developed MMIC VCO and Miller frequency divider operate properly as key components of the microwave PLL. When the associated components (loop filter, dc amplifier, etc.) are integrated on the GaAs substrate, an ultra-small-size microwave PLL is possible. This will be a potential candidate for local oscillators in space-borne transmitters, receivers, and radio relay systems.

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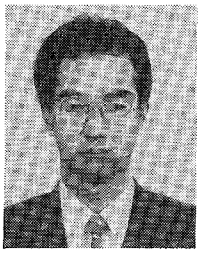

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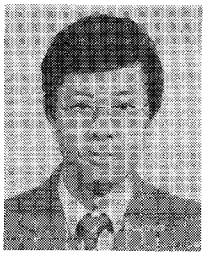

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